Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for processing an instruction within a processor, wherein the processor processes a plurality of types of interruptions, and wherein the processor comprises a plurality of register fields for indicating one or more conditions, statuses, and/or modes that are active within the processor, the method comprising:

executing an instruction within the processor;

receiving an interruption signal by the processor;

indicating whether the trap mode is active or inactive using a trap mode field within the processor, wherein a first trap mode field indicates that a single-step trap mode is active and wherein a second trap mode field indicates that a taken-branch trap mode is active;

in response to receiving the interruption signal, determining whether a trap mode is to remain active during interruption processing;

in response to a determination that the trap mode is to be deactivated during interruption processing, deactivating the trap mode; and

invoking an interruption handler to perform in interruption processing for the received interruption signal.

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Original) The method of claim 1 further comprising:

indicating whether a trap mode is to remain active during interruption processing using a trap mode conditioning field within the processor.

6. (Original) The method of claim 5 wherein a first trap mode conditioning field conditions activity of a single-step trap mode.

7. (Original) The method of claim 5 wherein a second trap mode conditioning field conditions activity of a taken-branch trap mode.

8. (Original) The method of claim 1 further comprising:
performing a trace operation prior to deactivating the trap mode.

9. (Original) The method of claim 1 further comprising:
reactivating the trap mode after interruption processing.

10. (Original) The method of claim 9 further comprising:
performing a trace operation after reactivating the trap mode.

11. (Currently Amended) A processor that performs operations specified by instructions fetched from a memory, the processor comprising:

means for maintaining a plurality of register fields for indicating one or more conditions, statuses, and/or modes that are present within the processor;

means for fetching instructions from memory;

means for executing an instruction within the processor;

means for receiving a plurality of types of interruptions;

means for indicating whether the trap mode is active or inactive using a trap mode field within the processor, wherein a first trap mode field indicates that a single-step trap mode is active and wherein a second trap mode field indicates that a taken-branch trap mode is active;

means for determining whether a trap mode is to remain active during interruption processing in response to receiving an interruption;

means for deactivating a trap mode in response to a determination that the trap mode is to be deactivated during interruption processing; and

means for invoking an interruption handler to perform interruption processing for a received interruption.

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Original) The processor of claim 11 further comprising:

means for maintaining a trap mode conditioning field within the processor to indicate whether a trap mode is to remain active during interruption processing.

16. (Original) The processor of claim 15 wherein a first trap mode conditioning field conditions activity of a single-step trap mode.

17. (Original) The processor of claim 15 wherein a second trap mode conditioning field conditions activity of a taken-branch trap mode.

18. (Original) The processor of claim 11 further comprising:

means for performing a trace operation prior to deactivating the trap mode.

19. (Original) The processor of claim 11 further comprising:

means for reactivating the trap mode after interruption processing.

20. (Original) The processor of claim 19 further comprising:

means for performing a trace operation after reactivating the trap mode.

21. (Currently Amended) A computer program product in a computer-readable medium for use in a data processing system for processing an instruction within a processor, wherein the processor processes a plurality of types of interruptions, and wherein the processor comprises a plurality of register fields for indicating one or more conditions, statuses, and/or modes that are active within the processor, the computer program product comprising:

means for executing an instruction within the processor;

means for receiving an interruption signal by the processor;

means for indicating whether the trap mode is active or inactive using a trap mode field within the processor, wherein a first trap mode field indicates that a single-step trap mode is active and wherein a second trap mode field indicates that a taken-branch trap mode is active;

means for determining whether a trap mode is to remain active during interruption processing in response to receiving the interruption signal;

means for deactivating the trap mode in response to a determination that the trap mode is to be deactivated during interruption processing; and

means for invoking an interruption handler to perform interruption processing for the received interruption signal.

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Original) The computer program product of claim 21 further comprising:

means for indicating whether a trap mode is to remain active during interruption processing using a trap mode conditioning field within the processor.

26. (Original) The computer program product of claim 25 wherein a first trap mode conditioning field conditions activity of a single-step trap mode.

27. (Original) The computer program product of claim 25 wherein a second trap mode conditioning field conditions activity of a taken-branch trap mode.

28. (Original) The computer program product of claim 21 further comprising:

means for performing a trace operation prior to deactivating the trap mode.

29. (Original) The computer program product of claim 21 further comprising:

means for reactivating the trap mode after interruption processing.

30. (Original) The computer program product of claim 29 further comprising:

means for performing a trace operation after reactivating the trap mode.

31. (New) The method of claim 1 further comprising:

determining the manner in which contention is resolved between trap mode processing and interruption processing based on a trap mode conditioning field of the processor status register.

32. (New) The method of claim 31 wherein a processor does not preserve the trap mode in any manner when an interruption occurs.

33. (New) The method of claim 31 wherein the processor suspends the trap mode when an interruption occurs.

34. (New) The method of claim 31 wherein the processor preserves the trap mode when an interruption occurs.

35. (New) The method of claim 31 wherein the trap handler immediately relinquishes execution control back to the interruption handler without performing any trace operations.

36. (New) The method of claim 31 wherein the trap handler generates a trace record when the trap handler is first invoked after the interruption handler has been entered, thereby providing a trace record at the start of the exception processing for the interruption.

37. (New) The method of claim 31 wherein the trap handler generates a trace record when the trap handler is invoked after the interruption handler has completed its processing operations, thereby providing a trace record at the end of the exception processing for the interruption.